

Please show your answers (and all work) on these sheets. Fold your paper the long way and write **your name** and **Homework 10** on the outside.

This problem tests your understanding of cache mapping. Assume that we are dealing with a processor in which:

- Memory is byte addressable.
- There are 2^{16} bytes of memory (that is, physical addresses are 16 bits wide).
- The L1 cache contains 2048 bytes with a 32 byte cache block (or line) size.
- The CPU is requesting the byte at the memory address 1110 1010 0110 1001 (in binary).

A. Suppose that the cache has **direct** organization. Give the values (in binary) of the three fields below used to locate the requested byte in the cache. If a field is not used in the direct cache organization, then write **unused**.

tag _____ set index _____ byte offset _____

B. Suppose that the cache has **four-way set associative** organization. Give the values (in binary) of the three fields below used to locate the requested byte in the cache. If a field is not used in the four-way set associative cache organization, then write **unused**.

tag _____ set index _____ byte offset _____

C. Suppose that the cache has **fully associative** organization. Give the values (in binary) of the three fields below used to locate the requested byte in the cache. If a field is not used in the fully associative cache organization, then write **unused**.

tag _____ set index _____ byte offset _____